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UNITED STATES PATENT APPLICATION

For

SELECTIVE COUPLING OF VOLTAGE FEEDS FOR BODY BIAS VOLTAGE IN AN INTEGRATED CIRCUIT DEVICE

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SELECTIVE COUPLING OF VOLTAGE FEEDS FOR BODY BIAS VOLTAGE IN AN INTEGRATED CIRCUIT DEVICE

FIELD OF THE INVENTION

Embodiments of the present invention relate to the manufacture and operation of integrated circuits. More particularly, embodiments of the present invention relate to selectively coupling voltage feeds to body bias voltage in an integrated circuit device.

RELATED APPLICATIONS

This Application is a Continuation-in-Part of co-pending commonly-owned United States Patent Application Serial No. 10/334,272 filed December 31, 2002, entitled "Diagonal Deep Well Region for Routing Body-Bias Voltage for MOSFETs in Surface Well Regions" to Pelham and Burr, which is hereby incorporated herein by reference in its entirety.

U. S. Patent number 6,489,224, entitled “Method for Engineering the Threshold Voltage of a Device Using Buried Wells”, to J. Burr, issued December 3, 2002, is hereby incorporated herein by reference in its entirety.

U. S. Patent number 6,303,444, entitled “Method for Introducing an Equivalent RC Circuit in a MOS Device Using Resistive Wells”, to J. Burr,

issued October 16, 2001, is hereby incorporated herein by reference in its entirety.

U. S. Patent number 6,218,708, entitled “Back-Biased MOS Device and Method”, to J. Burr, issued April 17, 2001, is hereby incorporated herein by reference in its entirety.

U. S. Patent number 6,091,283, entitled “Sub-Threshold Leakage Tuning Circuit”, issued July 18, 2000, is hereby incorporated herein by reference in its entirety.

U. S. Patent number 6,087,892, entitled “Target Ion/Ioff Threshold Tuning Circuit and Method”, to J. Burr, issued July 11, 2000, is hereby incorporated herein by reference in its entirety.

U. S. Patent number 6,048,746, entitled “Method for Making Die-Compensated Threshold Tuning Circuit”, to J. Burr, issued April 11, 2000, is hereby incorporated herein by reference in its entirety.

BACKGROUND

The generation of the physical layout of a semiconductor device having MOSFETs (metal oxide semiconductor field effect transistors) formed on a semiconductor substrate is a challenging task. An extensive amount of time and resources are spent during the creation of the physical layout. However, the effort can be reduced if new physical layouts utilize substantial portions of existing physical layouts. For example, a new physical layout comprising body-biased MOSFETs would consume fewer resources if an existing physical layout comprising MOSFETs without body biasing is utilized and modified according to the needs of the new physical design.

Unfortunately, this process of modifying the existing physical layout typically requires forming one or more additional routing layer(s) for the body biasing voltage(s) on the surface of the semiconductor device, creating a serious issue as the existing physical layout typically utilizes most if not all, of the available surface area. Additionally, it is highly desirable to accommodate the use of such a modified semiconductor device in applications designed for the unmodified (prior) semiconductor device. Consequently, it would be advantageous to provide a mechanism to vary the body voltage applied within such an integrated circuit.

<u>SUMMARY OF THE INVENTION</u>

An integrated circuit device having a body bias voltage mechanism is disclosed. The integrated circuit comprises a resistive structure disposed therein for selectively coupling either an external body bias voltage or a power supply voltage to biasing wells. A first pad for coupling with a first externally disposed pin can optionally be provided. The first pad is for receiving an externally applied body bias voltage. Circuitry for producing a body bias voltage can be coupled to the first pad for coupling a body bias voltage to a plurality of biasing wells disposed on the integrated circuit device. If an externally applied body bias voltage is not provided, the resistive structure automatically couples a power supply voltage to the biasing wells. The power supply voltage may be obtained internally to the integrated circuit.

In accordance with other embodiments of the present invention, a semiconductor device is disclosed. A first terminal for coupling a voltage to a body terminal of a metal oxide semiconductor is provided. In this embodiment, the body terminal is not coupled to a source or a drain of the metal oxide semiconductor.

More specifically, in accordance with still other embodiments of the present invention, a semiconductor device is provided, including a metal voltage rail coupled to a supply voltage. A first region of n well diffusion is provided

substantially below and coupled to the metal voltage rail. A second region of n well diffusion is coupled to a plurality of n well diffusion lines, wherein the n well diffusion lines couple a voltage of the second region of n well diffusion to n well regions of semiconductor devices. The first region of n well diffusion forms a desired resistance between the metal voltage rail and the second region of n well diffusion.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a top view of a pFET (or p-type MOSFET), in accordance with embodiments of the present invention.

Figure 2A illustrates an integrated circuit device in accordance with embodiments of the present invention.

Figure 2B illustrates a schematic of coupling between wells and power rails, in accordance with embodiments of the present invention.

Figure 3A illustrates an exemplary resistive structure, in accordance with embodiments of the present invention.

Figure 3B illustrates a cross-sectional view of an exemplary resistive structure, in accordance with embodiments of the present invention.

Figure 4A illustrates an exemplary resistive structure, in accordance with embodiments of the present invention.

Figure 4B illustrates an alternative resistive structure, in accordance with embodiments of the present invention.

Figure 4C illustrates a cross-sectional view of an exemplary resistive structure, in accordance with embodiments of the present invention.

Figure 5 illustrates a flow chart of a method for providing a body bias voltage in a semiconductor device, in accordance with embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention, selective coupling of voltage feeds for body bias voltage in an integrated circuit device, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be practiced without these specific details or with equivalents thereof. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

SELECTIVE COUPLING OF VOLTAGE FEEDS FOR BODY BIAS VOLTAGE IN AN INTEGRATED CIRCUIT DEVICE

Embodiments of the present invention are described in the context of design and operation of highly integrated semiconductor devices. It is appreciated, however, that elements of the present invention may be utilized in other areas of semiconductor operation.

Although the following description of embodiments of the present invention will focus on coupling a body-bias voltage to pFETs (or p-type MOSFETS) formed in surface N-wells via a conductive sub-surface region of N-type doping when a p-type substrate and an N-well process are utilized, embodiments in accordance with the present invention are equally applicable

to coupling a body-bias voltage to nFETs (or n-type MOSFETS) formed in surface P-wells via a conductive sub-surface region of P-type doping when an n-type substrate and a P-well process are utilized.

Figure 1 illustrates a top view of a pFET 50 (or p-type MOSFET) formed in an N-well 10 when a p-type substrate and an N-well process are utilized in accordance with an embodiment of the present invention. As depicted in Figure 1, pFET 50 comprises gate G, drain D (p-type doping), source S (p-type doping), and bulk/body B terminal 40. In particular, the bulk/body B terminal 40 is coupled to the N- well 10. Hence, a voltage applied to the bulk/body B terminal is received by the N-well 10. The N-well has an n-type doping. Regions of a semiconductor device that are doped with an n-type dopant have one type of conductivity while regions that are doped with a p-type dopant have another type of conductivity. Typically, various dopant concentrations are utilized in different regions of the semiconductor device.

It is to be appreciated that bulk/body B terminal 40 is coupled to terminal 30 via coupling 20. Coupling 20 conducts a signal, typically a substantially DC voltage generated, e.g., by body bias voltage source 60, from terminal 30 to bulk/body B terminal 40. Body bias voltage source 60 may be an on-chip voltage source or provided externally to an integrated circuit device.

Utilizing coupling 20, pFET 50 may be body-biased to influence its performance. More specifically, a bias voltage may be applied via coupling 20 to bulk/body B terminal 40. Without a body-biasing structure, the source S and bulk/body B terminal 40 are typically coupled together. With a body-biasing structure as described herein, the source S and bulk/body B terminals are not coupled together. Body biasing enables controlling a potential difference between the source S and bulk/body B terminals of the pFET 50, providing the ability to electrically tune the threshold voltage level of the pFET 50.

In accordance with embodiments of the present invention, terminal 30 may comprise a wide variety of well known structures. For example, terminal 30 may comprise an external package pin of a device comprising pFET 50. As an external pin, a voltage may be selectively coupled to the pin at an advantageous stage in a product development cycle, e.g., at final assembly by a jumper on a printed wiring board. By producing a semiconductor with a capability to provide a body bias voltage in this manner, users of the semiconductor device may take advantage of the benefits of body biasing while enjoying the ability to optimize the actual voltage later in the design process. It is appreciated that terminal 30 may be coupled to the same voltage rail as the source, yielding a MOS configuration similar to conventional devices lacking body biasing capabilities.

In the case of body biasing, the bulk/body B terminal receives a body-bias voltage Vn-well. As described above, the bulk/body B terminal represents a connection to the N-well 10. Thus, the body-bias voltage Vn-well is applied to the N-well 10.

Figure 2A illustrates an integrated circuit device 250 in accordance with embodiments of the present invention. Integrated circuit device 250 comprises a body bias distribution network 255. Body bias distribution network 255 distributes a bias voltage to body terminals, e.g., body terminal 40 of Figure 1, of semiconductor devices within integrated circuit device 250.

In accordance with embodiments of the present invention, a body bias voltage distributed by body bias distribution network 255 may be accessed from body bias voltage source 275, typically located off chip. An external body bias voltage source would typically be coupled via pin 290 to pad 280 to body bias distribution network 255.

In a case in which body bias voltage source 275 is not provided, or in a case in which body bias voltage source 275 suffers a failure, it is desirable for body bias wells to be maintained at a known voltage. An undefined voltage on a body bias well can result in unpredictable effects upon a threshold voltage of associated transistor devices, possibly leading to erroneous

operation, increased leakage current, latch up and/or damage to such transistor devices.

Accordingly, body bias distribution network 255 is also coupled to an internal voltage bus 270, e.g., a power supply voltage (Vdd) distribution bus. In a case in which body bias voltage source 275 is unavailable, the body bias wells are held at approximately the voltage of internal voltage bus 270, e.g., Vdd. In order to avoid a low resistance coupling, e.g., a "short," between body bias voltage source 275 and internal bus 270, which are typically at different voltages, the coupling between body bias distribution network 25 and internal bus 270 is made through a resistive structure 260. In general, resistive structure 260 should have a high resistance value compared to the path resistance of body bias distribution network 250.

Figure 2B illustrates a schematic 200 of a device for coupling between wells and power rails, in accordance with embodiments of the present invention. Voltage Vn-well 202 is a voltage applied to n wells of a semiconductor as described previously. Similarly, voltage Vp-well 201 is a voltage applied to p wells of a semiconductor. In general, to take advantage of decreased threshold voltage benefits of biased junctions, voltage Vn-well 202 should be greater than the supply voltage, Vdd, operating the semiconductor device. Frequently, such voltage is provided directly, for example via N well direct source 222, which can be, e.g., an on-chip voltage

source or external package pins coupled to an external voltage source. It is to be appreciated that embodiments in accordance with the present invention are well suited to forward biasing, e.g., Vn-well 202 less than the supply voltage, Vdd.

If a body bias voltage Vn-well 202 is not provided, e.g., by an on-chip voltage source or external package pin(s) coupled to an external voltage source, the body wells should not be left at an undefined voltage, e.g., "floating." An undefined voltage on a body bias well can result in unpredictable effects upon a threshold voltage of associated transistor devices, possibly leading to erroneous operation, increased leakage current, latch up and/or damage to such transistor devices.

In accordance with embodiments of the present invention, in such an absence of a defining voltage supply, body bias voltage Vn-well 202 can be biased to approximately the power supply by coupling N well structures to Vdd (or another suitable voltage) via resistive structure 220. A typical current in a deep n well body bias voltage distribution network can be about 1 μA. A typical resistance value for resistive structure 220 is approximately 1 kilo ohm in accordance with one implementation.

Similarly, voltage Vp-well 201 should be less than the low voltage, typically ground, coupled to the "ground" terminals of the semiconductor device to achieve a decreased threshold voltage. Frequently, such voltage is provided directly, for example via P well direct source 221, which can be, e.g., an on-chip ground connection or external package pins coupled to an external voltage source or ground. . It is to be appreciated that embodiments in accordance with the present invention are well suited to forward biasing, e.g., Vp-well 201 greater than ground.

Similarly, if a body bias voltage Vp-well 201 is not provided, e.g., by an on-chip voltage source or external package pin(s) coupled to an external voltage source, the body wells should not be left at an undefined voltage, e.g., "floating." An undefined voltage on a body bias well can result in unpredictable effects upon a threshold voltage of the associated transistor devices, possibly leading to erroneous operation, increased leakage current, latch up and/or damage to such transistor devices.

In accordance with embodiments of the present invention, in such an absence of a defining voltage supply, body bias voltage Vp-well 201 can be biased to approximately the power supply low voltage, typically ground, by coupling P well structures to ground (or another suitable voltage) via resistive structure 210. A typical current in a deep n well body bias voltage

distribution network can be about 1 μA. A typical resistance value for resistive structure 210 is approximately 1 kilo ohm in one embodiment.

As is explained in United States Patent Application Serial No. 10/334,272, referenced above, it is highly desirable to add body-biasing well structures to an existing chip design with minimum modification to the integrated circuit. Similarly, it would be highly desirable to add elements of coupling 200 to an existing chip design with minimum modification to the integrated circuit.

It is to be appreciated that coupling 200 provides an advantageous migration path for upgrading semiconductors from "non-body-biased" to a body-biased configuration, while minimizing impact to users of such products. For example, a circuit board can be designed for a first, "non-body biased" chip. By using elements of coupling 200, a second chip with biased N and P wells can be used in the same circuit board without modification to the circuit board. Resistive structures 201 and 202 can be used to couple existing voltage rails to the biasing wells, enabling the second chip to operate in a controlled manner.

Alternatively, additional pins, e.g., pins unused on the first chip, can be used to enable a new well-biasing function. For example, when the second

chip (with biasing wells) is installed into a circuit board, N well direct source 222 could be coupled to a bias voltage supply, e.g., external to the chip, while resistive structure 220 provides isolation between the Vdd and bias voltage supplies. Resistive structure 210 can provide similar isolation between a low bias voltage supply and ground.

Figure 3A illustrates a plan view of an exemplary resistive structure 220, in accordance with embodiments of the present invention. Resistive structure 220 is formed utilizing metallization, contacts, N+ diffusion, an N well and a deep N well structure. Resistive structure 220 can be formed in an area of a chip having an N well region with no devices located in the N well region.

Resistive structure 220 comprises metallization 320 coupled to a power voltage, e.g., Vdd. Metallization 320 corresponds schematically to terminal 220A of Figure 2. Deep N well 310 generally comprises a region of N well diffusion. Diffusion region 310A is substantially below metallization 330. Metallization 330 is coupled to metallization 320. By well known engineering techniques, the size, shape and separation of metallization 330 and diffusion region 310A can be designed to achieve a desired resistance, for example 1 kilo ohm. It is to be appreciated that substantially all of the resistance is achieved by diffusion region 310A. Diffusion region 310A can be designed with, for example, a length to width ratio of two to one. Such a regular shape allows for

computationally straightforward design of resistance values. It is appreciated, however, that embodiments in accordance with the present invention are well suited to a wide variety of shapes for diffusion region 210A.

Metallization 330 is coupled to diffusion region 310A by a plurality of contacts, e.g., contacts 351. Generally, only one set of contacts 351 – 354 will actually be used. By including provision for multiple sets of contacts in the design, the resistance of structure 220 can be determined empirically, and adjusted. For example, if only contacts 351 are constructed and used, the resistive path will have a higher resistance than if contacts 354 are utilized.

Diffusion region 310B is coupled to diffusion region 310A. Coupled to diffusion region 310B is a plurality of diffusion "lines" 340. Diffusion lines 340 couple resistive structure 220 to the various N well diffusion regions of the active devices of the semiconductor. It is to be appreciated that diffusion lines 340 are not coupled directly to diffusion region 310A. In this manner, diffusion region 310B corresponds schematically to terminal 220B of Figure 2. Diffusion region 310B is designed with a size and shape so as to allow coupling to diffusion lines 340 with a desirably low resistance.

Figure 3B illustrates a cross-sectional view of an exemplary resistive structure 220, in accordance with embodiments of the present invention. Figure 3B illustrates a section through contacts 351.

As conventional contacts typically do not couple to wells, metallization 330 is coupled via contacts 351 to N+ diffusion region 360. N+ diffusion region 360 is coupled to n-well 365. N-well 365 serves as a low resistance coupling to deep n-well 310A.

It is appreciated that Figures 3A and 3B illustrate embodiments in accordance with the present invention practiced in an n well semiconductor. More specifically, a resistive structure is formed between Vdd and lines 340 comprising a measured size of either n well or deep n well embedded in a p substrate. Embodiments in accordance with the present invention are well suited to practice in p well semiconductors. For example, a similar resistive structure can be formed embedded in an n substrate using a measured size of either p well or deep p well.

Figure 4A illustrates a plan view of an exemplary resistive structure 210, in accordance with embodiments of the present invention. Resistive structure 210 is formed utilizing a contact layer and a deep N well structure. Metallization 410A is coupled to a low voltage power rail, e.g., ground. Metallization 410A corresponds schematically to terminal 210A of Figure 2. N well diffusion region 410A is constructed around P well diffusion region 405. In this manner P well diffusion region 405 is isolated from the substrate except for

the portion at the bottom of the figure. The portion of P well region 405 at the bottom of the figure corresponds schematically to terminal 210B of Figure 2B.

Metallization 410A is coupled to P well region 405 by a plurality of contacts, e.g., contacts 451. Generally, only one set of contacts 451 – 454 will actually be used. By including provision for multiple sets of contacts in the design, the resistance of structure 210 can be determined empirically, and adjusted. For example, if only contacts 451 are constructed and used, the resistive path will have a higher resistance than if contacts 454 are utilized.

In accordance with well known engineering techniques, the size, shape and separation of metallization 410A and P well region 405 can be designed to achieve a desired resistance, for example 1 kilo ohm. P well region 405 can be designed with, for example, a length to width ratio of two to one. Such a regular shape allows for computationally straightforward design of resistance values. It is appreciated, however, that embodiments in accordance with the present invention are well suited to a wide variety of shapes for P well region 405. It is to be appreciated that substantially all of the resistance is achieved by P well region 405. The portion of P well region 405 at the bottom of the figure corresponds schematically to terminal 210B of Figure 2B.

Figure 4B illustrates an alternative resistive structure 210C, in accordance with embodiments of the present invention. Resistive structure

210C is formed utilizing a contact layer and a deep N well structure. Metallization 410B is coupled to a low voltage power rail, e.g., ground. Metallization 410B corresponds schematically to terminal 210A of Figure 2. N well diffusion region 460 is constructed around deep N well diffusion region 455. In this manner P well diffusion region 455 is isolated from the substrate except for the portion at the bottom of the Figure 4B.

According to well known engineering techniques, the size, shape and separation of metallization 410B and P well region 455 can be designed to achieve a desired resistance, for example 1 kilo ohm. It is to be appreciated that substantially all of the resistance is achieved by P well region 455.

Figure 4C illustrates a cross-sectional view of exemplary resistive structure 210, in accordance with embodiments of the present invention. Figure 4C illustrates a section through contacts 451.

As conventional contacts typically do not couple to wells, metallization 410A is coupled via contacts 451 to P+ diffusion region 470. P+ diffusion region 470 couples to p-well 405. N-well 410 and deep n-well 471 form a three-sided "box" around p well 405, forcing current to flow through the "bottom" of p-well 405 as shown in plan view in Figure 4A. P-well region 405 is isolated from the p-type substrate by n-well 410 and deep n-well 471. As p-well region 405 has a high resistance, forcing current to flow along the length of p-well 405 achieves a

desired resistance. It is to be appreciated that a cross section through a row of contacts for resistive structure 210C (Figure 4B) can be substantially similar.

It is appreciated that Figures 4A, 4B and 4C illustrate embodiments in accordance with the present invention practiced in an n well semiconductor. More specifically, a resistive structure is formed between Vss (ground) and a p substrate by isolating a p well of a measured length in an isolating conduit formed from n well and deep n well. Embodiments in accordance with the present invention are well suited to practice in p well semiconductors. For example, a similar resistive structure can be formed between Vss (ground) and an n substrate by isolating an n well of a measured length in an isolating conduit formed from p well and deep p well embedded in the n substrate.

Figure 5 illustrates a flow chart for a method 500 of providing a body bias voltage in a semiconductor device having a selectable coupling device, in accordance with embodiments of the present invention. In block 510, responsive to a coupling of an external body bias voltage to a designated pin of the semiconductor device, the external body bias voltage is coupled to body biasing wells of the semiconductor device.

In block 520, provided the external body bias voltage is not present, the body biasing wells of the semiconductor device are automatically supplied with an internal voltage of the semiconductor device through a resistance, e.g.,

resistive structure 220 of Figure 2B to provide the body bias voltage. In this novel manner, a semiconductor, e.g., a microprocessor comprising body-biasing wells, can advantageously be operated with or without an external body-biasing voltage applied. If an external body-biasing voltage is applied, the body bias can advantageously adjust a threshold voltage of transistor devices, e.g., to reduce leakage current. If no external body-biasing voltage is applied, the wells can be coupled to a power supply voltage, e.g., Vdd, such that the wells are at a fixed potential. In general, the coupling to a power supply voltage should be of sufficiently low resistance that the body biasing wells have a negligible effect on threshold voltages.

Embodiments in accordance with the present invention provide a circuit mechanism to selectively couple an external a voltage to body-biasing wells of a semiconductor device. Further embodiments of the present invention provide for the above mentioned solution to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

Embodiments in accordance with the present invention, selective coupling of voltage feeds for body bias voltage in an integrated circuit device, are thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention

should not be construed as limited by such embodiments, but rather construed according to the below claims.